CIRCUIT AND METHOD FOR REDUCING
SRAM STANDBY POWER

FIELD OF THE INVENTION

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This invention generally relates to electronic circuits, and more specifically to power reduction in semiconductor integrated circuits.

BACKGROUND OF THE INVENTION

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The continuing popularity of portable electronic devices presents manufacturers with contrary goals. Battery capacity is dependent upon battery size and weight. Thus portable electronic devices could be made to operate a longer time between battery changes or recharging if these devices included heavier batteries with greater capacity. On the other hand, portable

15   electronic devices would be more popular and more widely used if they were lighter. However, lighter weight translates into reduced battery capacity and reduced operating times. A large reduction in size of wireless telephones has taken place without significant reduction in operating times. While improvements in batteries have increased their capacity per unit weight, most of the improvement in operating time and reduction in device weight has come from improvements in

20   the power consumption of the electronics. Many improvements have taken place in integrated circuit manufacture that have reduced the amount of power consumed by the electronics. Additional improvements have taken place by selective powering of portions of the electronics. To a large degree much of the advantage of selectively powering a microcontroller unit or a digital signal processor have already been realized by current state of the art devices. Thus

25   manufacturers seek additional areas for power consumption reduction.

This additional area may be the system memory. Many portable electronic devices include substantial amounts of memory. Power savings may be gained by selectively powering either nonvolatile or volatile memory in respective active and standby operating modes. A circuit

30   and method for optimally switching between active and standby operating modes is described by

Haroun et al. in U.S. Pat. No. 6,151,262, which is incorporated herein by reference. Many circuit functions of volatile memory circuits such as dynamic random access memory (DRAM) and static random access memory (SRAM) may be suspended without loss of stored data. Moreover, some volatile memory in a wireless memory circuit may be used for computational storage, voice recognition, or other applications where data storage is only temporary. The process of fully powering these memory circuits typically requires much more time than that required for a memory access in the fully powered state. Thus, memory access time from a low power or standby state includes both the time required to power up the memory circuit and the normal access time. However, access times of these memories remains important, so it may not be feasible to completely shut the memory down to conserve power.

The inventors of the present invention have recently discovered that static random access memory cells power up in a state that minimizes leakage current. This phenomenon is explained with reference to TABLE I and Figures 4 and 5.

Normalized Cell Area	IDQ0 Mean	IDQ1 Mean	Power Up Mean	IDQ Ratio
0.84	3.65E-5	3.66E-5	4.30E-9	8500
0.89	6.33E-5	6.32E-5	6.00E-9	10542
0.92	6.02E-5	6.02E-5	4.10E-9	14683
0.92	9.00E-7	9.06E-7	3.90E-9	232
0.95	9.03E-7	8.10E-7	3.90E-9	220
1.00	5.80E-9	3.60E-9	2.90E-9	1.6

TABLE I

Referring to TABLE I, there are six rows representing different 6-T memory cells. These memory cells were fabricated by a complementary metal oxide semiconductor (CMOS) process. Mean entries in TABLE I are an average of measured data from fifty similar memory cells. The memory cells are arranged in order of normalized cell area as indicated in the left column. The top row, therefore, corresponds to the smallest cell area. The second column from the left is the

measured quiescent current when the memory cells store a true zero data state (IDQ0). The third

column from the left is the measured quiescent current when the memory cells store a true one

data state (IDQ1). The fourth column from the left is the quiescent current for the memory cells

of each row immediately after power up and before any data is written to the memory cells. The

5   far right column is a ratio of the average of quiescent currents IDQ0 and IDQ1 divided by the

quiescent current immediately after power up. The table shows that all except the last two rows

have approximately the same quiescent current for either a true one or a true data state. The

difference between IDQ0 and IDQ1 for the last two rows is slightly greater than for the previous

four rows. For example, IDQ0 for the last row is 5.80E-9 A and IDQ1 is 3.60E-9. Thus, the

10   IDQ1 current is about 60% greater than the IDQ0 current. By way of comparison, however, each

entry in the fourth column is significantly less than either of the corresponding IDQ0 or IDQ1

current. The quiescent current immediately after power up for each type of memory cells,

therefore, is significantly less than either IDQ0 or IDQ1. For example, the second and third rows

show more than four orders of magnitude less current in their respective power up states than the

15   mean of either IDQ0 or IDQ1. The fourth and fifth rows show more than two orders of

magnitude less current in their respective power up states than the mean of either IDQ0 or IDQ1.

Thus, the ratio in the far right column of average quiescent current (IDQ) to power up current in

the fourth column decreases significantly with increasing cell area as indicated in the first

column.

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Figure 4 illustrates a six-transistor (6-T) static random access memory cell. The memory

cell includes P-channel transistors 400 and 402 and N-channel transistors 404 and 406 connected

as a latch. N-channel pass gate transistors 408 and 410 couple bitline BL and complementary

bitline /BL to respective data terminals of the memory cell. The heavy dotted line of N-channel

25   transistor 406 indicates it has greater subthreshold leakage than N-channel transistor 404. This

greater leakage may be due to many different factors including inconsistent polycrystalline

silicon gate length, nonsymmetrical channel implants, nonsymmetrical source/drain implants, or

other factors. In fact, the leakage of N-channel transistor 406 may be as much as two orders of

magnitude or one hundred times greater than N-channel transistor 404. For example, a typical

30   transistor such as N-channel transistor 404 may have a subthreshold leakage current of 1 nA. By

way of comparison, a leaky transistor such as N-channel transistor 406 may have a subthreshold current of 10 nA. If residual data in a 256 K static random access memory with a 1.2 V power supply voltage leaves half of the data bits in a high leakage state, therefore, the memory array alone will dissipate 1.4 mW more power than if the entire array were in a low leakage state.

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During power up when the wordline WL is off, power supply voltage Vdd is applied to the sources of P-channel transistors 400 and 402. Current flows through the P-channel transistors to common drain terminals 412 and 414, respectively. Since N-channel transistor 406 has a greater leakage current than N-channel transistor 404, however, terminal 414 has a lower voltage

10   than terminal 412. As power supply voltage Vdd increases, the voltage at terminal 412 exceeds the threshold voltage of N-channel transistor 406 while the voltage at terminal 414 is still below the threshold voltage of N-channel transistor 404. Thus, N-channel transistor 406 becomes increasingly conductive and pulls terminal 414 even lower. This lower voltage at terminal 414 turns on P-channel transistor 400 and keeps N-channel transistor 404 off. This drives terminal

15   412 even higher, turning off P-channel transistor 402 and turning on N-channel transistor 406 even more. This regenerative effect continues as power supply voltage Vdd increases. When power supply voltage Vdd reaches a final value, therefore, terminal 414 is held at zero volts or ground and terminal 412 is held at power supply voltage Vdd. In this state, transistors 400 and 406 are both on. The leakage of the memory cell, therefore, is controlled by transistors 402 and

20   404, both of which are less leaky than transistor 406.

Referring now to Figure 5, there is another 6-T static random access memory cell. This memory cell is similar to the memory cell of Figure 4 except that the P-channel transistor 500 has a greater leakage current than P-channel transistor 502 as indicated by the heavy dotted line. N-

25   channel transistors 504 and 506 have approximately the same leakage current. When power supply voltage Vdd is applied during power up, therefore, P-channel transistor 500 produces a relatively higher voltage at terminal 512 than the voltage at terminal 514. As power supply voltage Vdd increases, this relatively higher voltage turns on N-channel transistor 506 while N-channel transistor 504 is still off. N-channel transistor 506, therefore, pulls terminal 514 even

30   lower, thereby turning on P-channel transistor 500 and holding N-channel transistor 504 off. The

increasingly conductive P-channel transistor 500 drives terminal 512 higher, thereby turning off P-channel transistor 502 and turning on N-channel transistor 506 even more. When power supply voltage Vdd reaches a final value, therefore, terminal 514 is held at zero volts or ground and terminal 512 is held at power supply voltage Vdd. In this state, transistors 500 and 506 are both

5   on. The leakage of the memory cell, therefore, is controlled by transistors 502 and 504, both of which are less leaky than transistor 500.

Memory cells of the prior art did not comprehend this pattern sensitive difference in quiescent current. Quiescent power dissipation of these prior art memory cell arrays was

10   determined by the existing data state of each memory cell during standby operation. Random data states of the memory cells might result in power dissipation similar to all-zero or all-one data states. This quiescent power dissipation, however, might be much greater than an all-zero or all-one data pattern. The worst case quiescent power dissipation of prior art memory arrays corresponds to a data state opposite the power up data state. This worst power dissipation may be

15   an order of magnitude greater than either the all-zero or all-one quiescent power dissipation.

The present invention describes a circuit and method to advantageously incorporate this power saving phenomenon in a portable electronic device such as a telephone handset, a handheld computer, a portable video game, or other battery powered device to greatly reduce standby current.

20   The reduced standby current in the static random access memory array prolongs battery life and operating time, resulting in less frequent battery recharging.

SUMMARY OF THE INVENTION

In accordance with a preferred embodiment of the invention, there is disclosed a method of operating a memory circuit. The method includes applying a first voltage to a power terminal of a memory cell having a first and a second data terminal. A data bit is stored in the memory cell. A second voltage different from the first voltage is applied to the power terminal. A third voltage is applied to the first and second data terminals. The first voltage is applied to the power terminal. The memory cell powers up in a state providing minimum leakage. Standby power is greatly reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features of the present invention may be more fully understood from the following detailed description, read in conjunction with the accompanying drawings, wherein:

Figure 1 is a block diagram of a wireless telephone which is an example of a portable electronic device which may advantageously employ the present invention;

Figure 2 is a block diagram of a static random access memory as may be used in the volatile memory circuit 148 of Figure 1;

Figure 3 is a circuit diagram of a portion of the timing and control circuit 200 of Figure 2;

Figure 4 is a schematic diagram of a 6-T memory cell of the static random access memory array 202 of Figure 2;

Figure 5 is a schematic diagram of another 6-T memory cell of the static random access memory array 202 of Figure 2;

Figure 6 is a schematic diagram of a memory cell of the static random access memory array of Figure 2 with precharge transistors of the present invention; and

Figure 7 is a timing diagram of the memory cell of Figure 6 illustrating operation of an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to Figure 1, there is a block diagram of a wireless telephone as an example of a portable electronic device which could advantageously employ this invention. Wireless telephone 100 includes antenna 102, radio frequency transceiver 104, baseband circuits 106, microphone 108, speaker 110, keypad 112, and display 114. The wireless telephone is preferably powered by a rechargeable battery (not shown) as is well known in the art. Antenna 102 permits wireless telephone 100 to interact with the radio frequency environment for wireless telephony in a manner known in the art. Radio frequency transceiver 104 both transmits and receives radio frequency signals via antenna 102. The transmitted signals are modulated by the voice/data output signals received from baseband circuits 106 on bus 120. The received signals are demodulated and supplied to baseband circuits 106 as voice/data input signals on bus 120. An analog section 130 includes an analog to digital converter 132 connected to microphone 108 to receive analog voice signals. The analog to digital converter 132 converts these analog voice signals to digital data and applies them to digital signal processor 140 via bus 120. Analog section 130 also includes a digital to analog converter 134 connected to speaker 110. Speaker 110 provides the voice output to the user. Digital section 106 is embodied in one or more integrated circuits and includes a microcontroller unit 142, a digital signal processor 140, nonvolatile memory circuit 146, and volatile memory circuit 148. Nonvolatile memory circuit 146 may include read only memory (ROM), ferroelectric memory (FeRAM), FLASH memory, or other nonvolatile memory as known in the art. Volatile memory circuit 148 may include dynamic random access memory (DRAM), static random access memory (SRAM), or other volatile memory circuits as known in the art. Microcontroller unit 142 interacts with keypad 112 to receive telephone number inputs and control inputs from the user. Microcontroller unit 142 supplies the drive function to display 114 to display numbers dialed, the current state of the telephone such as battery life remaining, and received alphanumeric messages. Digital signal processor 140 provides real time signal processing for transmit encoding, receive decoding, error detection and correction, echo cancellation, voice band filtering, etc. Both microcontroller unit 142 and digital signal processor 140 interface with nonvolatile memory circuit 146 via bus 144 for program instructions and user profile data. Microcontroller unit 142 and digital signal

processor 140 also interface with volatile memory circuit 148 via bus 144 for signal processing, voice recognition processing, and other applications.

5 Referring to Figure 2, there is a block diagram of a static random access memory as may be used in the volatile memory circuit 148 of Figure 1. The static random access memory includes a timing and control circuit 200 coupled to receive a clock enable signal CKE, a system clock signal CLK, and a read/write signal R/W. The timing and control signal generates internal control signals (not shown) to control read and write operations of the static random access memory. The timing and control circuit also generates a control signal S0 on lead 218 and a row counter address RCA

10 on bus 216 as will be explained in detail. Control signal S0 is applied to the control terminals of P-channel transistor 220 and N-channel transistor 222. The common drain terminal of P-channel transistor 220 and N-channel transistor 222 produces array power supply voltage VDA at lead 224. An address applied to bus 212 includes row and column address bits. The row address bits are applied to multiplex circuit 214. The column address bits are applied to column decoder circuit 206.

15 Multiplex circuit 214 selectively applies one of the external row address bits on bus 212 or the row counter address RCA on bus 216 to row decoder circuit 204 in response to the logic state of control signal S0. A high logic state of control signal S0 will apply row counter address RCA to the row decoder circuit 204. Alternatively, a low logic state of control signal S0 will apply the row address on bus 212 to the row decoder circuit 204. The row decoder circuit activates a wordline in response

20 to the row address from multiplex circuit 214, thereby selecting a row of memory cells from the static random access memory array 202. The column decoder circuit 206 selects a column of memory cells in response to the column address bits on bus 212. A data bit at the intersection of the selected row and column produces data to output circuit 208 during a read operation. Alternatively, the data bit at the intersection of the selected row and column receives data from input circuit 210

25 during a write operation.

Turning now to Figure 3, there is a schematic diagram of a portion of timing and control circuit 200 of Figure 2. The timing and control circuit includes an edge detector circuit formed by inverter 300, delay circuit 302, and NOR gate 304. The output of NOR gate 304 is coupled to the S input of S-R flip flop 306. The R input of S-R flip flop 306 is coupled to receive clock counter carry

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signal CCY on lead 310. The Q output of S-R flip flop is applied to AND gate 308 together with clock signal CLK. The output of AND gate 308 is applied to clock counter circuit 312. Clock counter carry signal CCY on lead 310 is applied to the S input of S-R flip flop 314. The Q output of S-R flip flop 314 produces control signal S0 on lead 218, which is applied to AND gate 320

5   together with clock signal CLK. The output of AND gate 320 is coupled to row counter circuit 318. Row counter circuit 318 produces row counter address signal RCA on bus 216 and row counter carry signal RCY on lead 316.

In normal operation, the timing and control circuit 200 receives a high level clock enable

10   signal CKE. This high level produces a low level output from NOR gate 304 at the S input of S-R flip flop 306. The Q output of S-R flip flop 306, therefore, remains low as will be described in detail. The low level of the Q output S-R flip flop 306 produces a low level output from AND gate 308 so that clock counter circuit 312 does not receive clock signal CLK or generate clock counter carry signal CCY. Thus, control signal S0 at the Q output of S-R flip flop 314 remains low. This

15   low level of control signal S0 applied to an input of AND gate 320 produces a low level output so that row counter circuit 318 does not receive clock signal CLK. Thus, row counter carry signal RCY remains low and row counter circuit 318 does not produce row counter address signal RCA.

The static random access memory circuit enters a standby operating mode when clock

20   enable signal CKE goes low. This high-to-low transition produces a high level pulse output from NOR gate 304. The low level of clock enable signal CKE is inverted by inverter 300 and delayed for a time Δt determined by delay circuit 302. After this delay, a high level signal from delay circuit 302 produces a low output from NOR gate 304. The high level pulse from NOR gate 304 sets a high level Q output from S-R flip flop 306. This high level Q output is applied to AND gate 308,

25   thereby passing clock signal CLK to clock counter circuit 312. Clock counter circuit 312 includes a predetermined number of stages which count cycles of clock signal CLK until a grace period has elapsed. Overflow of clock counter circuit 312 at the end of the grace period produces a clock counter carry signal CCY on lead 310. The high level of counter carry signal CCY sets control signal S0 at the Q output of S-R flip flop 314 high. After one more cycle of clock signal CLK, the

high level of counter carry signal CCY also resets S-R flip flop 306. This additional cycle of clock signal CLK applied to clock counter circuit 312 resets counter carry signal CCY to a low level.

The high level of control signal S0 on lead 218 is applied to multiplex circuit 214 (Figure 2) to select row counter address signal RCA on bus 216 as previously described. Control signal S0 is also applied to AND gate 320, thereby passing clock signal CLK to row counter circuit 318. In response to clock signal CLK, row counter circuit 318 produces a sequence of row address signals on bus 216. These row address signals are subsequently applied to row decoder circuit 204 (Figure 2) to sequentially activate each wordline in the static random access memory array 202. When row counter circuit 318 has completed the sequence of row addresses, the counter overflows and produces row counter carry signal RCY on lead 316. Row counter carry signal RCY resets control signal S0 at the Q output of S-R flip flop 314 low, thereby resetting multiplex circuit 214 to pass row address bits from bus 212 on a subsequent memory access. The low level of control signal S0 applied to AND gate 320 also ceases application of clock signal CLK to row counter circuit 318.

Turning now to Figure 6, there is a static random access memory cell of the present invention. The memory cell includes P-channel transistors 600 and 602 and N-channel transistors 604 and 606. The sources of P-channel transistors 600 and 602 are coupled to receive array power supply voltage VDA on lead 224. N-channel pass gate transistors 408 and 410 couple memory cell data terminals 612 and 614 to bitline BL and complementary bitline /BL terminals, respectively. The bitline BL and complementary bitline /BL terminals are coupled to a respective column of memory cells by respective N-channel pass gate transistors. Other memory cells in the column are not shown to preserve clarity in the following explanation. Each column of memory cells includes a respective pair of N-channel precharge transistors 616 and 618 coupled between bitline BL and complementary bitline /BL and ground, respectively. The control terminals of N-channel precharge transistors 616 and 618 are coupled to receive control signal S0 on lead 218.

Referring now to Figure 7, operation of the memory cell of Figure 6 will be explained in detail. During active operation prior to time t_0, array power supply voltage VDA is high and control signal S0 is low. In this active mode, the static random access operates in a manner similar to

memories of the prior art. When clock enable signal CKE (Figures 2 and 3) goes low, however, the static random access memory enters a standby mode of operation. This high-to-low transition of clock enable signal CKE initiates a grace period as previously explained. The duration of this grace period is preferably determined by clock counter circuit 312 (Figure 3). After expiration of the

5   grace period, control signal S0 goes high at time t_0. The high level of control signal S0 turns off P-channel transistor 220 and turns on N-channel transistor 222 (Figure 2), thereby driving array power supply voltage VDA to zero volts or ground. Other peripheral circuits such as row 204 and column 206 decoder circuits continue to receive power from power supply voltage Vdd. Control signal S0 also selectively applies row counter address RCA on bus 216 to row decoder circuit 204. Finally,

10   control signal S0 turns on N-channel precharge transistors 616 and 618 and corresponding N-channel transistors for each column of the static random access memory. Row counter circuit 318 (Figure 3) then produces a sequence of row addresses beginning at time t_1. The active wordline at time t_1 turns on N-channel pass gate transistors 408 and 410, thereby coupling data terminals 612 and 614 to bitline BL and complementary bitline /BL, respectively. Bitline BL and complementary

15   bitline /BL are coupled to ground through N-channel precharge transistors 616 and 618, respectively, in response to the high logic state of control signal S0. Thus, the data terminals 612 and 614 of the memory cell are coupled to ground. This advantageously precharges both data terminals of the memory cell and each memory cell connected to the active wordline WL to ground. This equalized precharge state eliminates any residual charge imbalance at the data terminals 612

20   and 614 of the memory cell. Row counter circuit 318 (Figure 3) continues to address each wordline in the array until time t_2, when the row counter circuit generates row counter carry signal RCY. Row counter carry signal RCY then resets S-R flip flop 314 and produces a low level control signal S0 at time t_3. The low level of control signal S0 also turns off N-channel precharge transistors 616 and 618 (Figure 6) and corresponding N-channel transistors for each column of memory cells. The

25   low level of control signal S0 turns off N-channel transistor 222 and turns on P-channel transistor 220 (Figure 2), thereby restoring array power supply voltage VDA to a high level. As array power supply voltage VDA increases, each memory cell of the static random access memory array powers up in a respective lowest leakage state as previously explained. This low leakage state forms a unique bit pattern within each static random access memory array. The low leakage of this unique

30   state advantageously reduces standby power of the static random access memory. Moreover, for an

exemplary 256 K static random access memory, an average power of approximately 25 μW for less than 3 μS is required to reset the static random access memory array to a low leakage state. This power consumption is negligible by comparison to the previously discussed 8 mW of power dissipation for half of the memory array bits in a high leakage state.

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While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. For example, N-channel

10 transistors might precharge data terminals to a different reference voltage than ground. This may be accomplished by an existing bitline precharge circuit of the memory array. In another embodiment of the present invention, the bitline precharge circuit may precharge the bitlines to one reference voltage for normal circuit operation and to a different reference voltage prior to power up. Alternatively, a single N-channel transistor might be used to simply equalize the voltage of bitline

15 BL and complementary bitline /BL. Furthermore, the unique bit pattern might be stored in a separate nonvolatile memory and rewritten to the static random access memory after expiration of the grace period.

In view of the foregoing discussion, it is intended that the appended claims encompass any

20 such modifications or embodiments.